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The Reversible Universal Gate and realization of basic gates in Quantum Dot Cellular Automata

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Abstract—Quantum Cellular Automata (QCA) is new nan- otechnology which recently has become one of the top six emerging technologies with the potential for applying in building future computers. This technology is a realization of the circuit design at the Nano-scale. The basic logic in QCA does not use voltage level for logic representation but instead it represents binary state by polarizing the electrons on the Quantum Cell which is the basic building block of QCA. Reversible logic design is a well-known model in the world of digital computation, and in this paper we are presenting realization of some basic logic gates in QCA using the Reversible Universal Gate (RUG).

Index Terms—QCA, Quantum Dots, Reversible gates, Basic gates

1 Introduction

Over the past three decades, the microelectronics sector has witnessed unprecedented reductions in device size and processing time. Moore's law, which states that the number of integrated devices on a chip will double approximately every 18 months, has been followed by this pattern for quite some time. It has been a herculean effort to keep up with this exponential development trajectory, necessitating significant advancements in all elements of integrated circuit (IC) fabri- cation to allow manufacturers to simultaneously reduce device size and expand chip size while maintaining acceptable yields. The field effect transistor (FET) has been the go-to device for high levels of integration since the 1970s. Modern FETs have come a long way since their infancy, but they continue to serve as a current switch similar to Konrad Zuse's mechanical relays from the 1930s.In order to continue scaling, FETs will run into fundamental effects at gate lengths below 0.1 mm [1]. The microelectronics industry may be able to keep up with the increasing demand for smaller and smaller devices by shifting from the FET-based paradigm to one based on nanostructures. In this case, the benefits of feature size reduction are exploited rather than fought. The quantum-dot cellular automata (QCA) developed by Lent et al is a nonstructural paradigm that uses arrays of connected quantum dots to realise Boolean logic operations. QCA's benefits come from the small size of the dots, the simpler interconnection, and the extremely low power-delay product, all of which allow for exceptionally high packing densities. Within $1mm^2$ of space, a full adder can be implemented using QCA cells with dots 20 nm in diameter [2].

Four quantum dots arranged in a square and connected by tunnel barriers constitute a fundamental QCA cell. By tunnelling between the dots, electrons can move about inside the cell but are unable to escape. If two extra electrons are added to the cell, they will be attracted to the dots on opposing corners due to Coulomb repulsion. As can be seen in Fig. 1, two polarizations of the ground state exist that are equivalent in energy. These can be thought of as the logical states 0 and 1.

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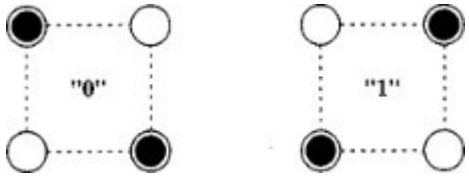

Fig. 1. The two alternative ground-state polarizations are depicted in this basic four-dot QCA cell.

Because of the strong coulombic interaction between electrons, the cell can rapidly transition between these two polarizations. Fig. 2(a) depicts the simplest form of QCA array, a linear arrangement of cells. Given that the cells are capacitively connected to one another, it follows that a line in which all cells are equally polarised represents the ground state. The electrons are as far apart as they can be, resulting in the least amount of energy. In order to use the line, the input must be supplied at its left end, which forces the first cell out of its degenerate ground state and into a single polarization. Now that the first and second cells in the line have switched polarities and there are two electrons close together, the line is in a higher energy state, and all succeeding cells must flip their polarization to reach the new ground state. There can be no metastable state in a row of cells where just a small fraction of the cells undergo a phase transition. One of the greatest benefits of QCA devices is the paradigm shift that has allowed for greatly easier connectivity [2]. Having the cells just talk to their immediate neighbours eliminates the need for lengthy connecting links. Inputs are sent to the outermost cells of the system, which then perform the computation and produce results that are sent to the outermost cells of the QCA array. Using the QCA paradigm, computing can be thought of

as computing with the system's ground state. By strategically arranging the cells, it is possible to represent the answer to a computing problem as the configuration of electrons in their ground state. Computation then becomes the process of introducing inputs that excite the system and allowing it to settle back to a new ground state. Different outputs are generated for different inputs [3].

For given parameters, there is one and only one ground state of the system that represents the solution. The basic logic operations AND, OR, and NOT can be implemented by arranging QCA cells in specific ways, which allows for the issue of combinational logic to be mapped onto a QCA system. If you look at Fig. 2(b), you'll see an inverter (or a NOT). It is shown that the input to this inverter is first separated into two lines of cells, then brought back together at a cell that is rotated 45 degrees from the two lines. The cell must be oriented at 45 degrees from the two lines for an inverter to function. In practice, the majority gate topology depicted in Fig. 2(c) is used to create AND and OR gates. The polarization state of the central cell is decided by a majority vote from the gate's three inputs. The propagated polarisation is the state of the central cell. Choose the AND or OR operation by programming one of the inputs. As an OR gate if the input is a logic 1, and as an AND gate otherwise. Therefore, any combinational logic operations can be realised with majority gates and inverters. It is conceivable to use QCA cells for general-purpose computing because they may be used to implement memory as well [3]. Further explanation is required for the fan-out structure used in the inverter, as depicted in Fig. 2(d). All of the cells in both branches must flip in order to reach the new ground state of the system when the input of one of these structures is reversed. The input cell flip does not provide enough energy to flip all the cells in the system, leading to a metastable condition in which not all of the cells have flipped. This is not the system's ground state, but it may persist for a long time and produce incorrect results when used in a calculation. If the cells are switched in a quasi-adiabatic fashion, the system is maintained in its instantaneous ground state, preventing the emergence of any metastable states,

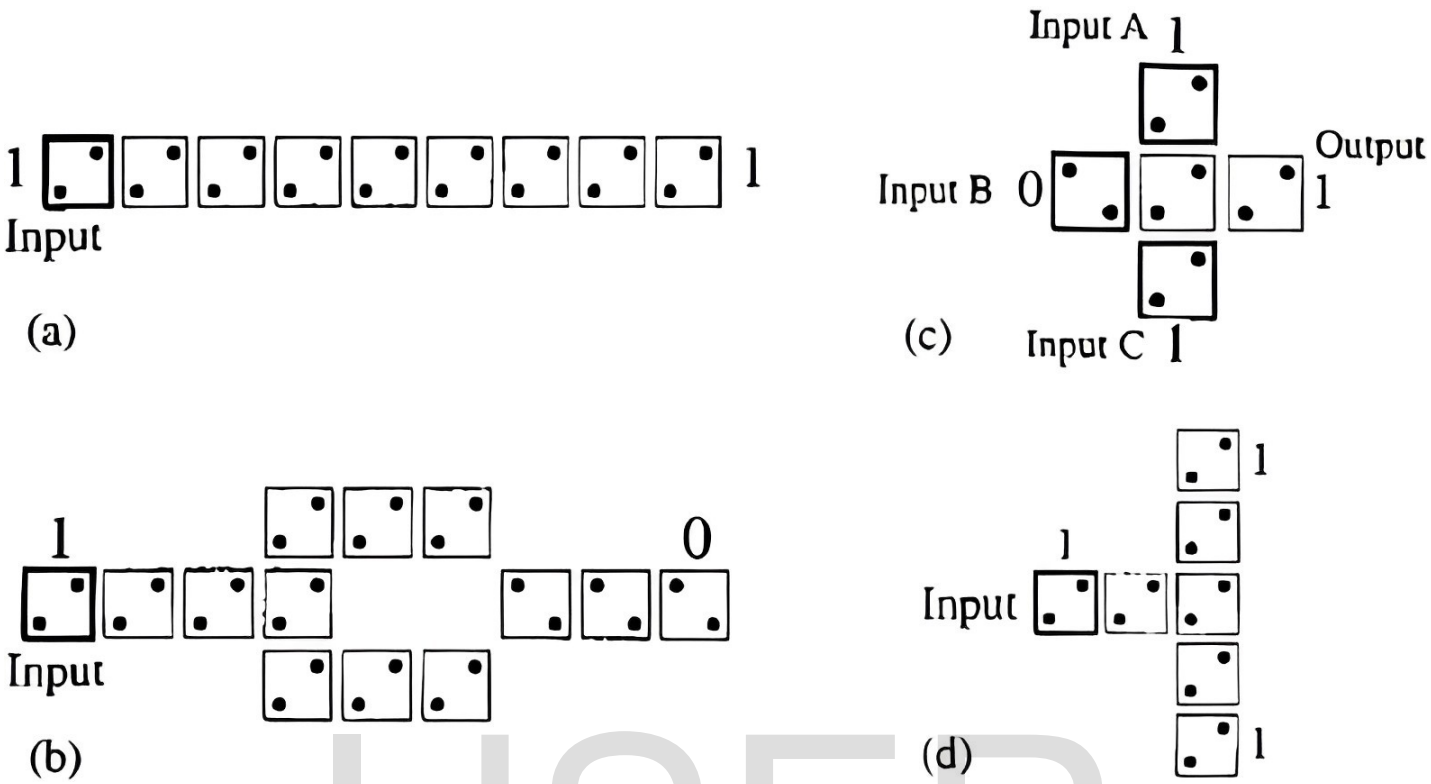

Fig. 2. 2. (a) Line of QCA cells. (b) QCA inverter. (c) QCA majority gate. (d)Fanout

and the switching process can proceed without incident. Previous publications provide specifics on quasi-adiabatic switching. Both semiconductor and metallic QA devices support quasi-adiabatic switching [4].

QCA can be used to realise both sequential and combinational designs. The clocking zone partition scheme is typically used in QCA circuits and systems. To create columns, designs are typically divided into different clocking zones along a single dimension, such as the X-axis (as zones). Clocking and pipelining necessitate designs to keep sets of four adjacent zones at all times (as per the four phases, or Switch, Hold, Release, and Relax). A cell's Switch phase occurs when its excess electrons become polarised by the surrounding cells, giving it a clear binary value. In the Hold phase, interdot barriers are increased, preventing electron polarity switching. During the Release phase, inter dot barriers are lowered and cellular polarity is lost. There is no inter dot barrier or cellular influence in the Relax phase. For example, consider the cell in Fig. 1, which shows the cell at each of its four clock phases. As can be seen in Fig. 4, a QCA design's clocking is applied by a signal-generating circuitry that is embedded beneath the surface. The electric field necessary to alter the tunnelling barrier of all cells in the region is produced by this signal (adiabatic switching) [5].

In addition to the well-known kinds of power dissipation in a logic circuit—static and dynamic power consumption—Landauer (In 1961) identified information loss as another cause of energy loss in a logic circuit. Logical reversible computing is accomplished by constructing a one-to-one map- ping between input and output vectors in the circuit. Whereas in reversible systems in quantum technology, the fan-out is not possible, the bijective quality can be shown via (1-to- 1) mapping. The Majority Voting (MV) function in QCA technology cannot be undone logically due to the loss of information in the minority input. The

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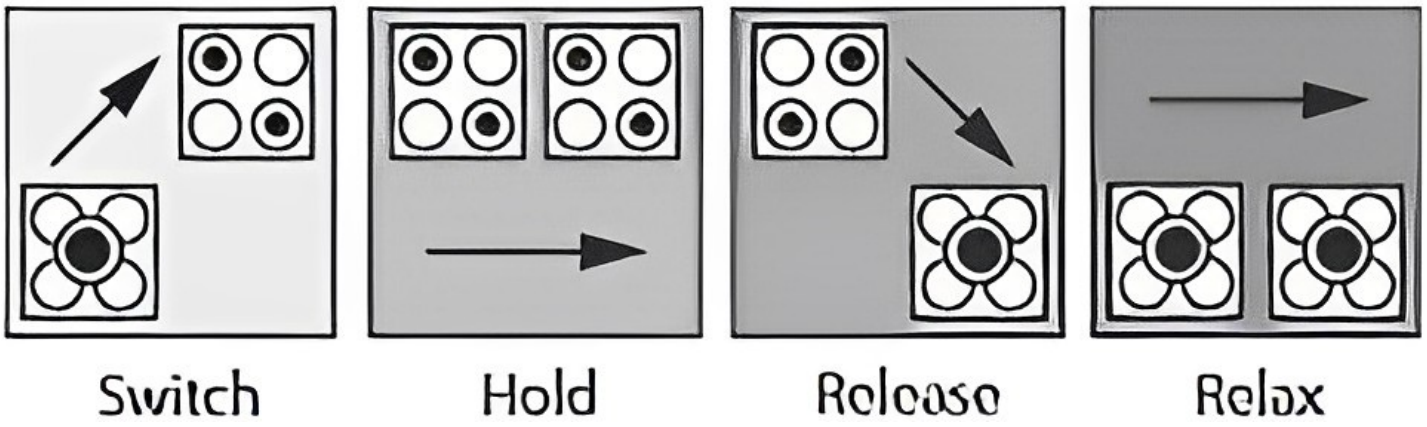

Fig. 3. QCA clock phases

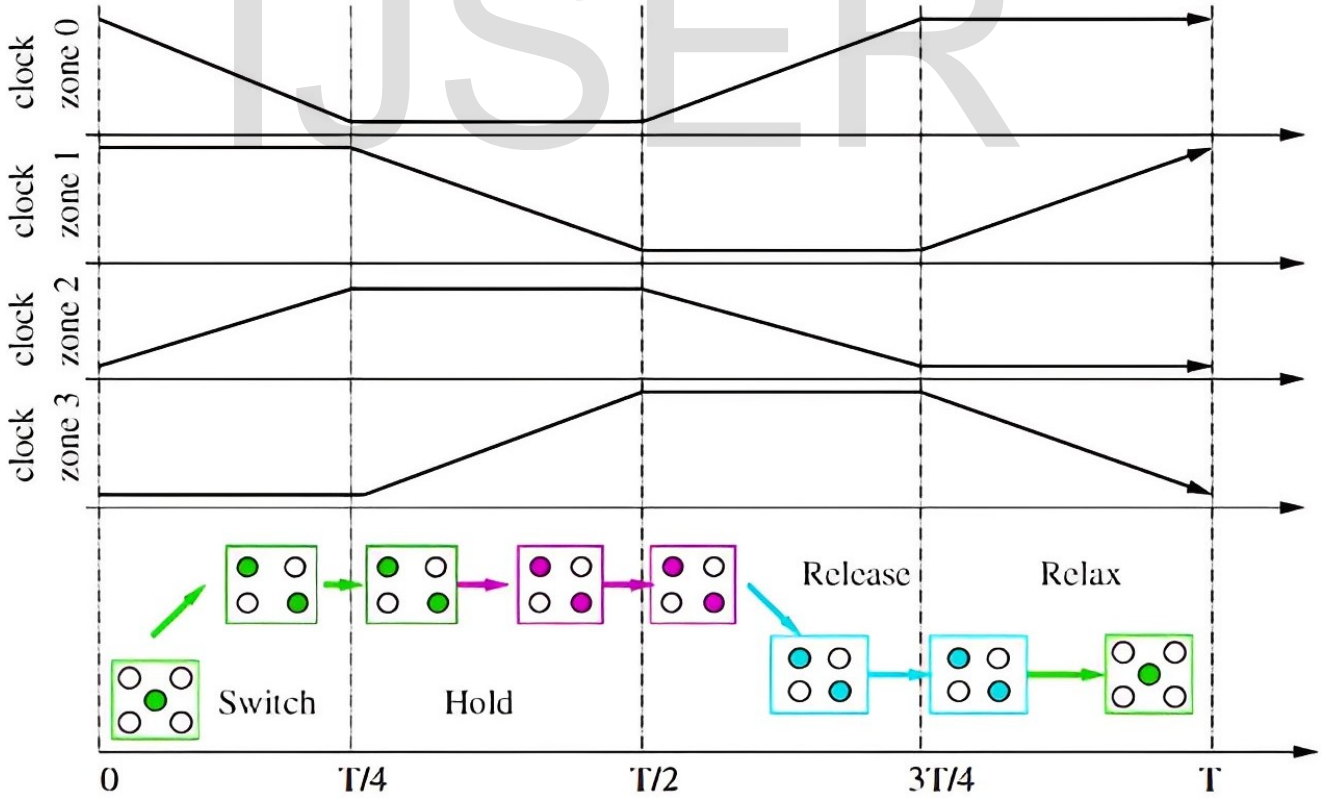

Fig. 4. Four-phased signal for clocking, adiabatic switching

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error occurs while trying to calculate something. In reality, reversible computing can make use of Bennett clocking, which can be viewed as an alternative clocking configuration in QCA [6]. In light of this, the QCA can be used to accomplish reversible computing in practice. QCA circuits, which can include MV and fan-out devices, have a significantly lower energy dissipation per switching event and are not constrained by physical constraints. Bennett timing has been directly calculated to get this result. We can deduce that the fan-out is optional in QCA technology for generating RGs. A Bennet clocking method has been implemented in the QCA Timing section [6].

2 Related Work

Certainly, there has been a lot of research done in this field of quantum dots and no doubt there will be a lot of research done in future as well. Many researchers have worked on QCA trying to build better designs for the basic gates and there has also been work done on building some reversible gates. Research have been done to perfect these designs and measure their efficiency of them with respect to power dissipation and energy consumption. Numerous designs have been proposed for the gates ranging from AND, OR to Toffoli, Fredkin, Peres and so on [7]. There has been work done on the Reversible Universal Gate as well where multiple implementations of it in QCA is put forward which is not the most efficient work out there. Some designs are very huge thus increasing the cell area and cell count but there is little to no work done on how this particular gate can be used to realize the basic gates. The research that we have come across proposes the circuit designs of the said realizations but fails to provide the QCA implementation of it. Hence we took it upon ourselves to refer to these circuit diagrams and implement the realization in the QCA domain [7].

3 The RUG Gate

The Reversible Universal Gate is one of the reversible logic that is widely used In QCA to implement many functions and to build other components like the adders and subtractors, Over the years there has been a lot of development in the domain of reversible logic, and every researcher trying to design more efficient models of the gates. We have taken inspiration from such research and further contributed to the work of reversible logic by modifying the design of the RUG gate and making it more efficient by conserving the cell count and hence the cell area.

In theory, the RUG gate is a 3 input 3 output device that has the following circuit design as shown in Fig. 6. It takes input A,B,C which further generates 3 unique functions which are reversible in nature to get back the unique input combination. The truth table for this gate is shown in Fig. 7

The design that we are proposing is quite efficient in terms of the cell count and cell area and we believe because of this the power dissipation and energy consumption are also very minimal. Our proposed design is shown in Fig. 8. As seen in the design it is seen that the structure has used crossovers and bridges to accomplish the design. Several majority gates and inverter gates have been used as well. The output waveform simulation of this design is shown in Fig. 9 which can be further cross-verified with the truth table in Fig. 7. The output of the simulation has 2 kinds of waveforms, the inputs are represented in blue while the outputs are represented in yellow. In this design, we have made use of only 3 clocks, unlike the designs which were proposed earlier which used 4. The cell count of this design is 91 while the cell area is $0.08um^2$.

4 Basic Gates

Inputs A, B, C, D, etc. are all examples of possible inputs to a digital logic gate, although there is often only one digital output (Q). By connecting or cascading many logic gates together, it is possible to create a logic gate function

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Input: a given determination of reversible function
Output: a synthesized RG using of the MG

1. Make the MSM given that the number of function inputs
2. For every fi $(i = 1:m$ m: the number of function outputs)
3. { For every of MSMs made
4. { Detect the most analogous column to the feature of the main function (MF) in MSM
5. Detect the most analogous column given that features of columns combination in MSM.
6. Detect the most analogous feature between the MF and columns of inputs.
7. Iterate Lines 4 & 5 for supplementary function (fi), again.
8. Iterate Lines 4 & 5 of the algorithm for all methods explained in [22] and keep the results.
9. Apply the method of C-K-map to the MF and keep the result.
}
}.
10. Utilize majority expression made in every fi for synthesis other fj $(j \neq i)$
11. Chose results between outputs to the most common expressions.
12. For decreasing the number of NGs, utilize the below specifications

$Maj(a', b', c')' = Maj(a, b, c)$

Fig. 5. An algorithm of the synthesis of a reversible function

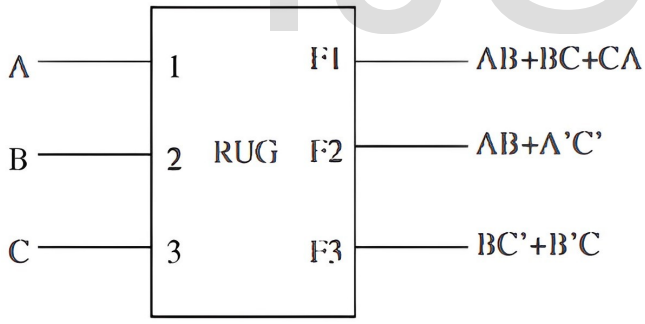

Fig. 6. Circuit design of RUG gate

A B C	F1	F2	F3
0 0 0	0	1	0
0 0 1	0	0	1
0 1 0	0	1	1
0 1 1	1	0	0
1 0 0	0	0	0
1 0 1	1	0	1
1 1 0	1	1	1
1 1 1	1	1	0

Fig. 7. Truth table of RUG gate

with an unlimited number of inputs, as well as combination and sequential type circuits and new logic gate functions. The Digital Logic Gate is the fundamental element of all microprocessor-based systems and digital electrical circuits. The AND, OR, and NOT gates of a digital computer execute logical operations on binary values.

Logic "1" and Logic "0," often known as HIGH and LOW, or TRUE and FALSE, are the only two voltage levels or states allowed in digital logic design. Boolean algebra and truth tables use the binary digits "1" and "0" to represent these two possible outcomes.

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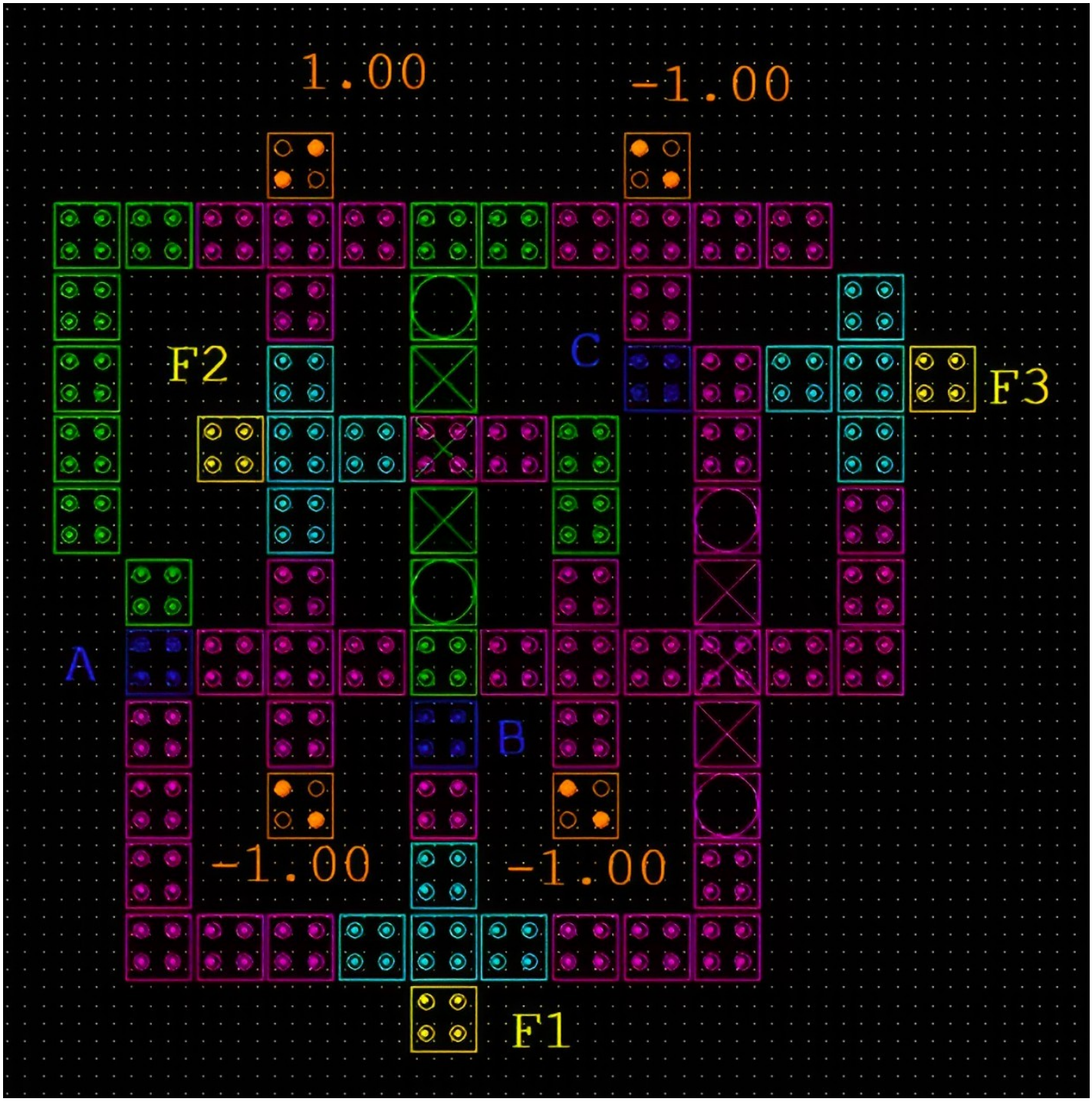


Fig. 8. RUG Gate in QCA

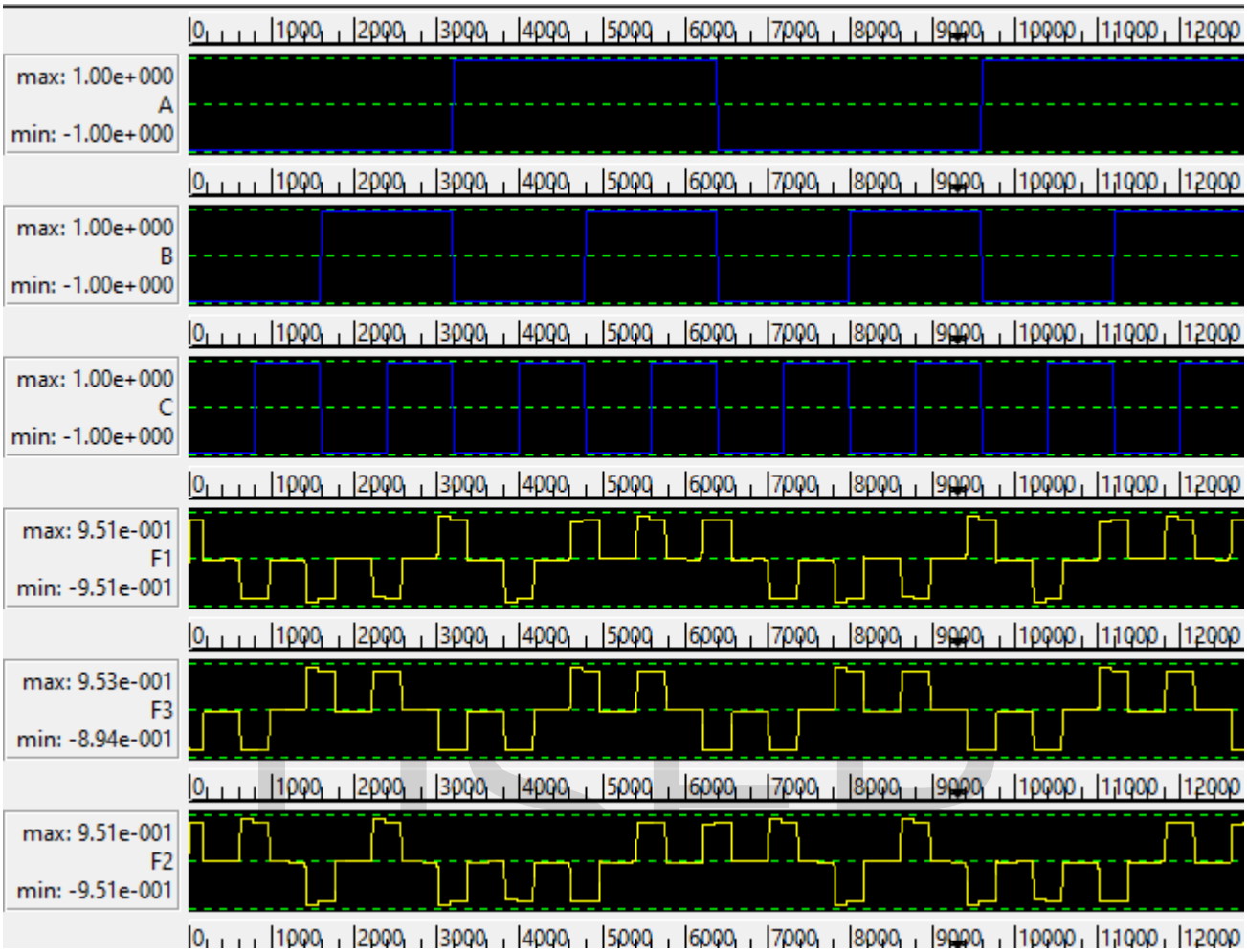


Fig. 9. Output simulation of RUG gate

The RUG gate has been further employed in our work to realize the design of basic gates which can be used in various circuit designs to implement more complicated architecture like ALU, Adders and Subtractors. We have made use of our design to realize the basic gates and we were successful in the implementation.

4.1 AND Gate

A high output (1) is produced by the AND gate electrical circuit if and only if all inputs are also high. The AND operator is represented by a dot (.) in the expression A.B. It's important to keep in mind that it's common to leave this dot out, e.g., AB. The block diagram and its corresponding truth table of AND gate is shown in Fig. 10 and the QCA realization of this gate using RUG gate is shown in Fig. 15 while its simulation output in Fig. 16

4.2 OR Gate

The electrical OR gate produces a high output (1) if any two of its inputs are high. The AND operation is represented by a minus (-), while OR is shown by a plus (+). The block diagram and its corresponding truth table of OR gate is shown in Fig. 11 and the QCA realization of this gate using RUG gate is shown in Fig. 17 while its simulation output in Fig. 19

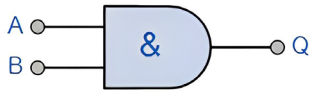
Symbol	Truth Table		
 2-input AND Gate	B	A	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A.B	Read as A AND B gives Q		

Fig. 10. Block diagram and Truth table of AND gate

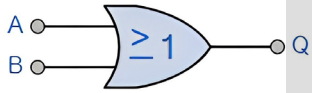
Symbol	Truth Table		
 2-input OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression Q = A+B	Read as A OR B gives Q		

Fig. 11. Block diagram and Truth table of OR gate

4.3 NOT Gate

The output of the NOT gate, an electrical circuit, is the inverse of the input. It's often called a "inverter," too. The NOT A output signifies an inverted value of the input variable, A. This is also represented by the symbol A', which resembles the letter A but has a vertical bar added to it. The block diagram and its corresponding truth table of NOT gate is shown in Fig. 12 and the QCA realization of this gate using RUG gate is shown in Fig. 20 while its simulation output in Fig. 18

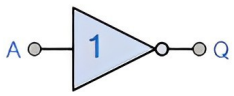
Symbol	Truth Table	
 Inverter or NOT Gate	A	Q
	0	1
	1	0
Boolean Expression Q = not A or $\overline{A}$	Read as inverse of A gives Q	

Fig. 12. Block diagram and Truth table of NOT gate

4.4 EXOR gate

A 'Exclusive-OR' gate is a logic circuit with a high output if one of its two inputs is high, but not both. To symbolise EOR, we use a plus sign () enclosed in a circle. The block diagram and its corresponding truth table of EXOR gate is shown in Fig. 13 and the QCA realization of this gate using RUG gate is shown in Fig. 21 while its simulation output in Fig. 23

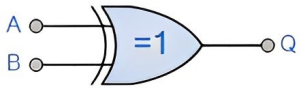
Symbol	Truth Table		
 2-input Ex-OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A ⊕ B	A OR B but NOT BOTH gives Q		

Fig. 13. Block diagram and Truth table of EXOR gate

4.5 EXNOR Gate

With an output that is ordinarily at logic level "1" and going "LOW" to logic level "0" when ANY of its inputs are at logic level "1," the "Exclusive-NOR Gate" is essentially a mixture of the Exclusive-OR gate and the NOT gate with a truth table similar to the regular NOR gate. The block diagram and its corresponding truth table of EXNOR gate

is shown in Fig. 14 and the QCA realization of this gate using RUG gate is shown in Fig. 24 while its simulation output in Fig. 22

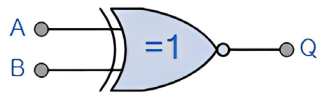
Symbol	Truth Table		
 2-input Ex-NOR Gate	B	A	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression $Q = \overline{A \oplus B}$	Read if A AND B the SAME gives Q		

Fig. 14. Block diagram and Truth table of EXNOR gate

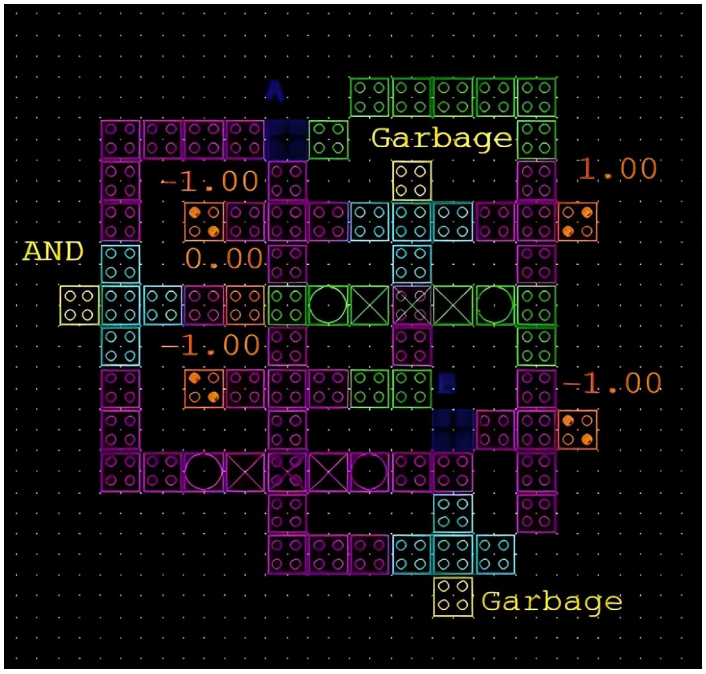


Fig. 15. AND gate realization using RUG gate

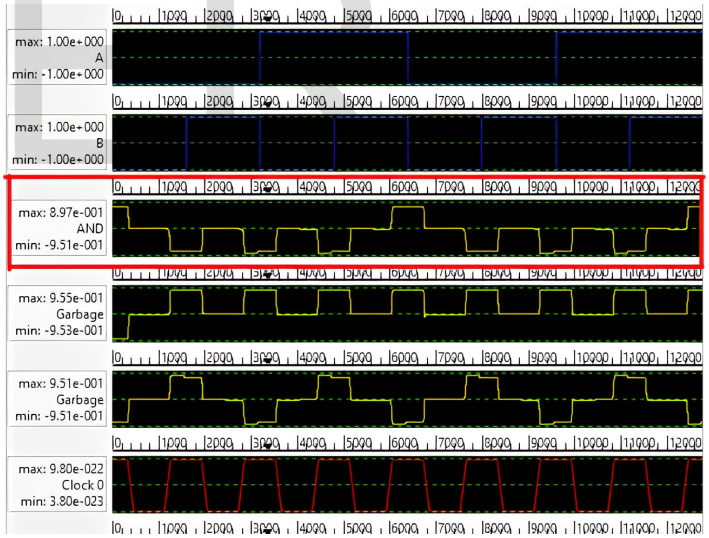


Fig. 16. AND gate simulation output

4.6 QCA Designs and Outputs

This section provides the implemented the QCA design of the basic gates using the RUG fate and its output simulation for further verification using the truth table of the respective gate.

5 Conclusion

As a novel approach for designing highly scalable logic cir- cuits at the Nanoscale, quantum-dot cellular automata (QCA) are gaining traction in the industry. Since logic gates form the backbone of most digital circuits, it is crucial to have designs that are fast, simple, and take up little space. This study demonstrates how a single Reversible Universal Gate can serve as a realisation of both the basic and reversible gates (RUG). The output waveforms of the proposed circuits were successfully simulated, and the findings were double- checked against the truth tables. This paper presents the RUG, a reversible QCA logic gate structure that satisfies the purpose of a universal reversible gate in a power-efficient logic design. It has been demonstrated that the RUG based QCA cir- cuits are more efficient than designs based on conventional reversible gates in terms of the number of logic gates and trash outputs. This low-cost, high-density RUG capability is going to be crucial in multiprocessor CMPs. Reports of RUG's successful implementation of symmetric functions and bench- marks are encour-

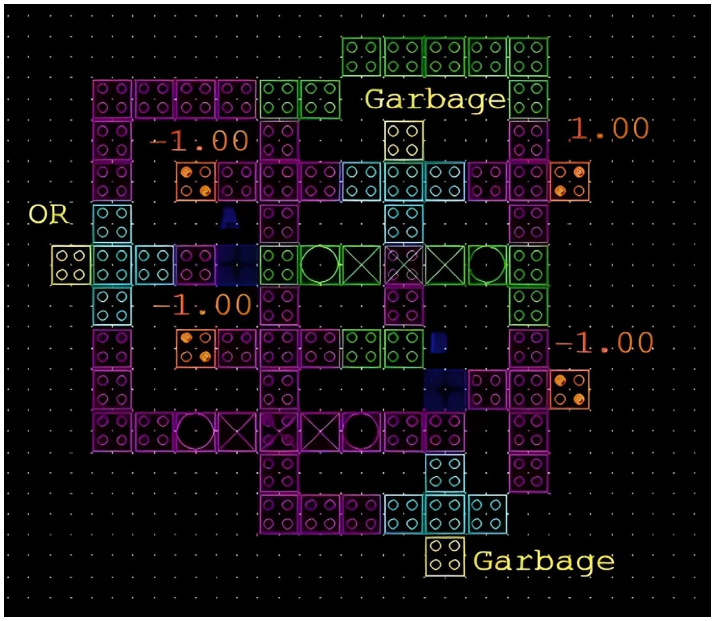


Fig. 17. OR gate realization using RUG gate

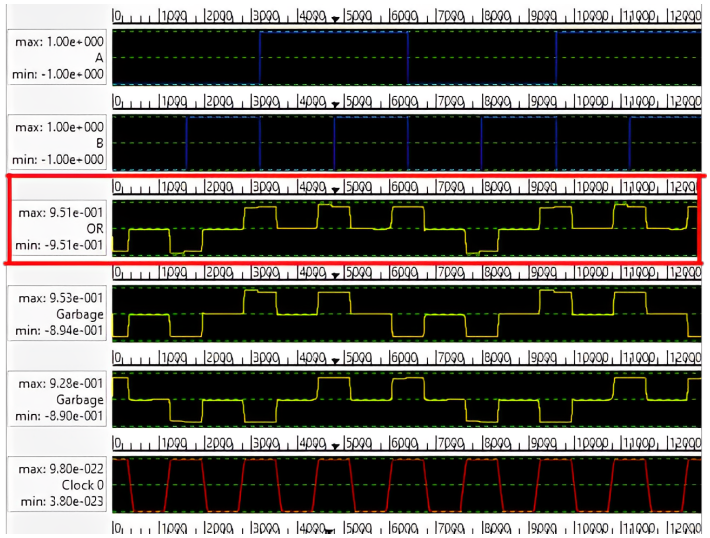


Fig. 19. OR gate simulation output

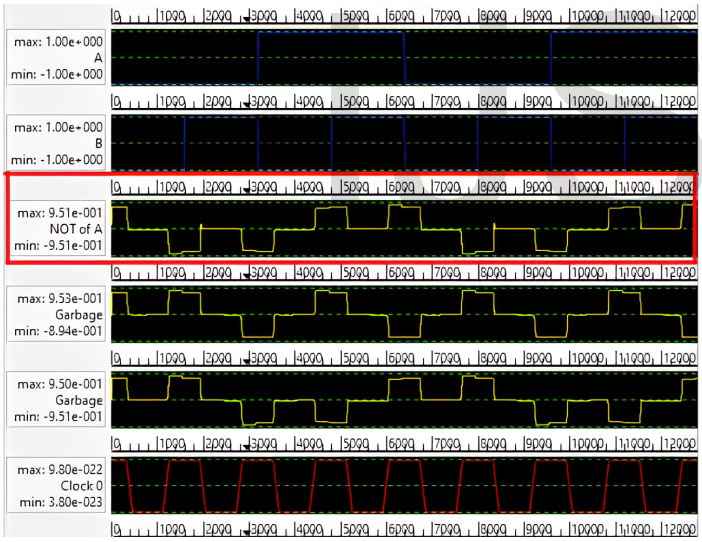


Fig. 18. NOT gate simulation output

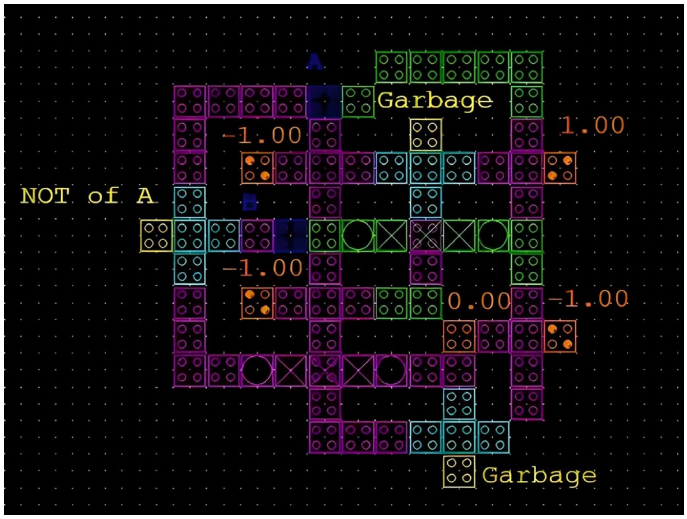


Fig. 20. NOT gate realization using RUG gate

aging. In doing so, it proves that low-power QCA designs may be implemented with any reversible gate supporting universal, majority, and XOR functions. Addition- ally, we offer a novel method for simultaneous error detection in re- versible logic circuits. Online testing of reversible circuits using comparatives is ruled out. Both the number of cells and their total area are assumed to decrease during the ex- periment.

This research also proposes a reversible circuit that uses less cell space while remaining highly effective.

In our endeavour to realize the basic gates using the RUG, we were unsuccessful in implementing the univer- sal gates, NAND and NOR but successful in implementing every other basic gate with a design most effective to the best of our knowledge.

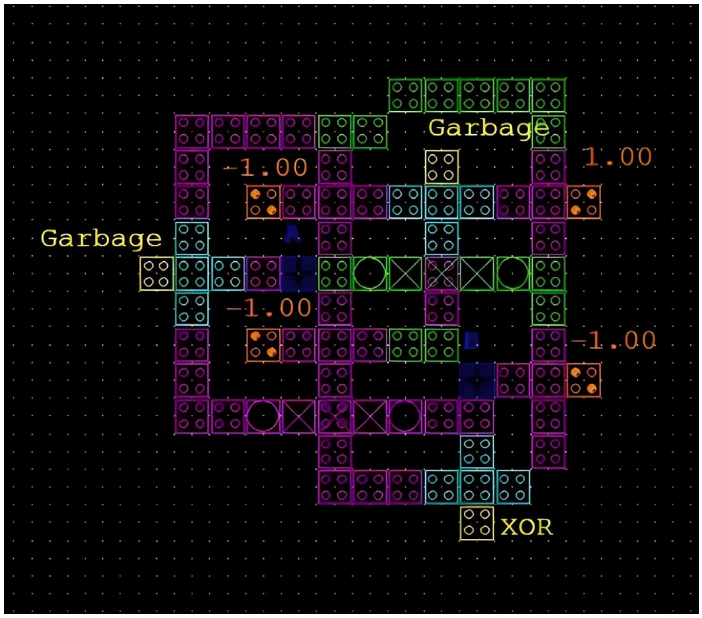


Fig. 21. EXOR gate realization using RUG gate

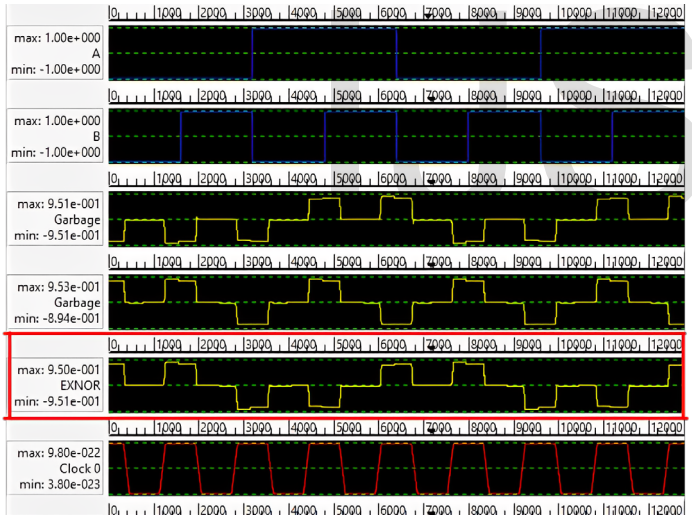


Fig. 22. EXNOR gate simulation output

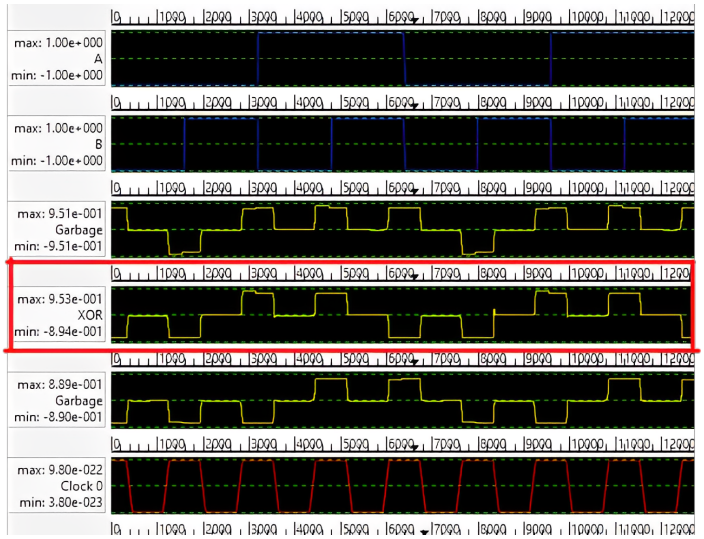


Fig. 23. EXOR gate simulation output

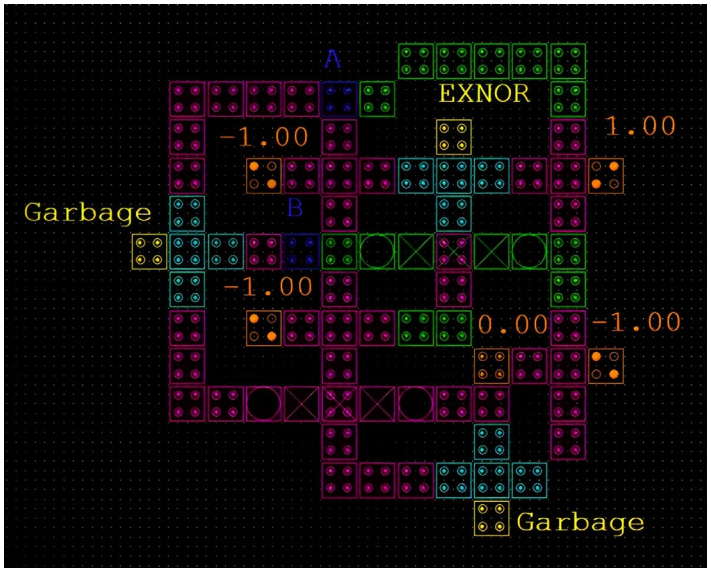


Fig. 24. EXNOR gate realization using RUG gate

6 Future Work

There certainly is a lot og scope for the further development in this domain. The design can be further optimised to be more power efficient and occupy less space and the work of realization of basic gates that we have proposed is just the beginning of the efficient use of reversible gates. To progress further, more work can be done in realization of the universal gates like NAND and NOR by using RUG and then using these gates to essentially build Adders and Subtractors which have a lot of bio medical applications. One step further would be the development of ALU by purely using RUG gates and deploying them in real time to make the best use of it while also making usre that it is energy efficient.

Furthermore what can be done is to calculate the exact power consumption and energy dissipation in these circuits to tally and compare woth the traditional designs ther by

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takinganother step closer to the part of efficiency. At the end of the day we work to make sure that there is advancement in quantum field and this can only happen one step at a time.

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